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**Spatial Atomic Layer Deposition of Zinc Oxide:
An Alternative Approach to Printed Electronics**

Much of the effort toward making a microelectronics technology out of organic semiconductors has been driven by a desire for “printable” or “printed” electronics. Such printed electronics—involving simplified and high-speed processes—would enable a new generation of low-cost and ubiquitous applications with a variety of new form factors. A difficulty often encountered is that the needs of a simplified process such as printing require the semiconductors, dielectrics, and electrode materials to have ink-like properties as well as electronic ones. In this talk, we will introduce an approach to printed electronics that separates the ink-like requirements from the active materials requirements.

In the system discussed in this talk, the deposition of active materials is by an atmospheric pressure, roll-compatible process called spatial atomic layer deposition (S-ALD), and the materials deposited are metal oxides. We will demonstrate that this new deposition process maintains the desirable attributes of atomic layer deposition such as excellent film quality and thickness control, while also achieving high throughput and ease of use at temperatures at and below 200˚C. In addition to depositing good-quality thin-film transistor layers, S-ALD allows for selective-area patterning during deposition. This allows additive patterning, in which a growth-inhibiting layer is printed and the oxides then only deposit where desired. Electrical properties of S-ALD-grown thin-film transistors, such as mobility above 20 $cm^2$/V-s, high on/off ratios, and good uniformity of the deposited layers will be demonstrated, along with good stability with respect to bias stress. The combination of patterning and good properties provides a promising approach to printed electronics.