Effects of Bias Stress in Organic Thin-film Transistors

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Organic transistor technology holds the promise of large-area flexible electronics and integration of various sensors and actuators on a single substrate [1,2]. However current-voltage (I-V) characteristics of organic transistors are known to change with the application of prolonged voltages [3]. Such change, termed the bias-stress effect, leads to operational instability which limits the usable lifetime of the circuit. The bias-stress effect must be understood and minimized to enable the use of organic transistors in functional applications. In this work, we present a method to accurately measure the bias-stress effect and a model that predicts the effect at different stress conditions. The model provides physical insight into the mechanisms causing the bias-stress effect and an estimate on the expected lifetime of the transistor. It also provides a means to determine the operation regime that minimizes the bias-stress effect.

To measure the bias-stress effect and no other degradation effects, we characterize pentacene OTFTs that have no measurable change due to storage in nitrogen ambient. We demonstrate that the after-stress I-V characteristics can be accurately described by the initial I-V characteristics and a shift in applied gate voltage, ΔV. Based on this observation, we characterize the bias-stress effect with ΔV. We measure ΔV at different gate and drain bias (V_{SG} and V_{SD}) and stress times. Measurements with different V_{SD} at fixed V_{SG} stress show that ΔV decreases with increasing drain bias or current, indicating that gate field and channel carriers are responsible for the stress effect, not drain current. We report that ΔV saturates at 14 V independent of the V_{SG} stress. We propose a simple carrier trapping rate model that results in a stretched-exponential equation that accurately describes the observed ΔV behavior with respect to stress times. The model suggests that the bias-stress effect is caused by trapping of the channel carriers. The bias-stress effect saturates due to a constant number of trap sites unlike in a-Si:H TFTs where the trap sites are continually created until there are no more channel carriers [4]. The saturation of the bias-stress effect independent of the V_{SG} stress is reported for the first time in organic transistors.

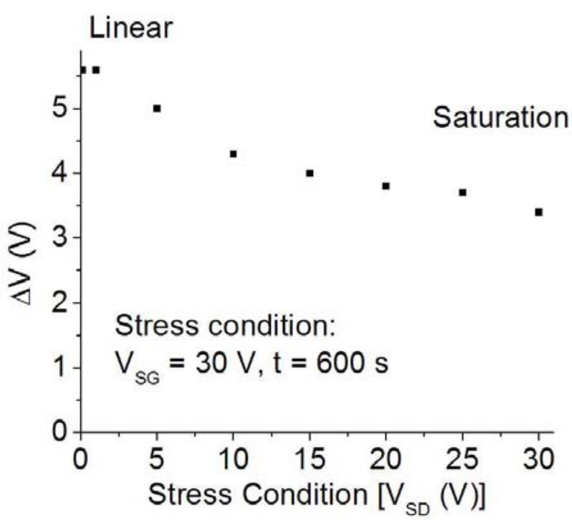

Figure 1 – ΔV vs stress V_{SD} at t = 600 s. The V_{SG} during stress was held at 30 V. The induced ΔV decreases with increasing V_{SD}.

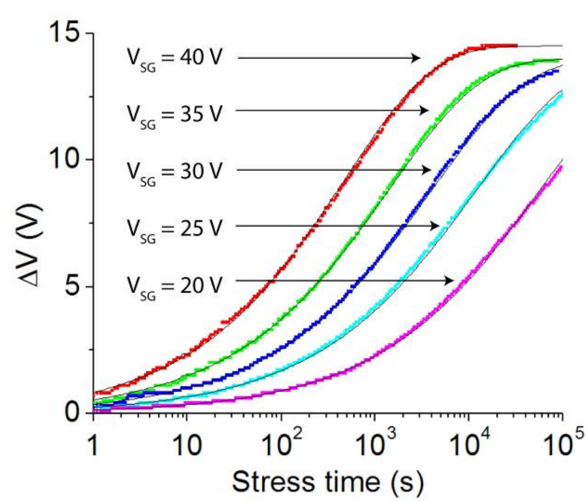

Figure 2 – Measured stress time dependence of the induced ΔV for different gate bias-stress conditions (colored dots) and the stretched-exponential fit made to the data (solid lines). Each stress condition has fifty data points per decade.

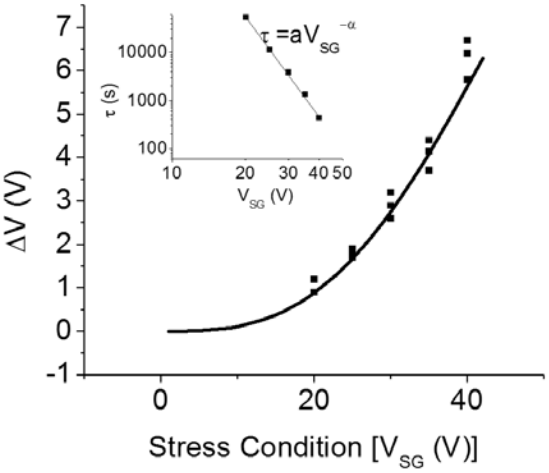

Figure 3 – ΔV vs stress V_{SG} after 100 seconds of stress. The V_{SD} during stress was held at 1 V. Each stress condition was repeated three times, each time on a fresh device. The solid line is ΔV predicted by the model. (inset) log-log plot of τ vs V_{SG}.

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